REMARKS

In the Office Action, the Examiner noted that Claims 1-20 are pending in the application and that Claims 1-2, 4-6, 8, 10-11, and 13-20 are rejected. The Examiner objected to Claims 3, 7, 9, and 12. By this response, Claims 1-20 continue without amendment. In view of the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Objections

The Examiner has objected to dependent Claims 3, 7, 9, and 12 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicants thank the Examiner for indicating allowable subject matter, but believe independent claims 1 and 6, from which these dependent claims depend, are allowable over the prior art of record for the reasons set forth below. Thus, Applicants contend that Claims 3, 7, 9, and 12 should distinguish over the prior art of record, since each claim depends from independent Claims 1 or 6. Therefore, Applicants respectfully request that the objection to Claims 3, 7, 9, and 12 be withdrawn.

II. Rejection Of Claims Under 35 U.S.C. §102

The Examiner rejected Claims 1-2, 4-6, 8, 11, 13, 15, and 20 as being anticipated by Song (United States Patent 5,321,825, issued June 14, 1994). The rejection is respectfully traversed.

More specifically, the Examiner stated that Song teaches use of a lock field in a register associated with a shared memory. (Office Action, p. 2). The Examiner further stated that Song discloses controlling access to the shared memory among a plurality of processors in response to the state of the lock field in the register. (Office Action, p. 3). Applicants respectfully disagree.

Song discloses a processing system having two processors, two lock buffers respectively coupled to the two processors, and a shared memory. The processors,

lock buffers, and shared memory are coupled to a common bus. (See Song, col. 4, lines 17-37; FIG. 1). Each of the lock buffers includes fields for controlling access to portions of the shared memory by a respective one of the processors. (Song, col. 4, line 59 through col. 5, line 18). That is, a given processor cannot access a particular portion of the shared memory unless the state of the lock field in its associated lock buffer allows such access. Once a given processor obtains access, the processor causes its lock buffer to update the fields of the other lock buffer for the other processor. (Song, col. 8, lines 23-42).

In view of the foregoing, Song does not teach each and every element of Applicants' invention recited in claim 1. Namely, Song does not teach or suggest providing a semaphore and "controlling access among the plurality of processors to the first portion of the memory in response to the state of the semaphore." (Applicants' Claim 1). That is, Song does not teach or suggest controlling access to a shared memory among multiple processors based on the state of a single semaphore or lock buffer ("the semaphore"). Rather, Song controls access to a shared memory among the processors based on states of multiple lock buffers, one for each processor. A given lock buffer in Song controls access to the memory by only a single processor. In Song, a processor does not check the status of lock buffers for other processors, but rather only checks its own lock buffer. While a given lock buffer updates the fields of other lock buffers once granting access to is associated processor, multiple lock buffers are still required to arbitrate access to the memory among all of the processors. If one of the lock buffers in Song is omitted, arbitration among the processors will fail. This is in contrast with Applicants' invention, where access to a shared memory by a plurality of processors is controlled based on the state of a single semaphore ("the semaphore"). Controlling access to a memory among a plurality of processors using multiple lock buffers, as disclosed by Song, does not teach or suggest controlling access to a memory among processors using a single semaphore, as recited in Applicants' Claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481,

485 (Fed. Cir. 1984). Since Song does not teach or suggest controlling access among multiple processors to a memory in response to state of a single semaphore, Song does not teach each and every element of Applicants' Claim 1. Claims 6, 13, and 15 recite features similar to those of Claim 1 discussed above. In particular, Claim 6 recites, among other features, "associating a semaphore with the task data" and "controlling access among the plurality of processors to the task data in response to a state of the semaphore." Claims 13 and 15 recite, among other features, "a semaphore circuit" and "means for controlling access among the plurality of processors to the first portion of the memory in response to a state of the semaphore circuit." For the same reasons set forth above, Song does not teach each and every element of Applicants' Claims 6, 13, and 15.

Claims 2, 4-5, 8, 11, and 20 depend, either directly or indirectly, from Claims 1, and 15 and recite additional features therefor. Since Song does not anticipate Applicants' invention as recited in Claims 1 and 15, dependent Claims 2, 4-5, 8, 11, and 20 are also not anticipated and are allowable. Therefore, Applicants contend that Claims 1-2, 4-6, 8, 11, 13, 15, and 20 are not anticipated by Song and, as such, fully satisfy the requirements of 35 U.S.C. §102.

III. Rejection of Claims Under 35 U.S.C. §103

The Examiner rejected Claims 16-18 as being unpatentable over Song in view of Trimberger (United States patent 6,573,748, issued June 3, 2003). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Song does not disclose the system being embedded within a programmable logic device (PLD). (Office Action, p. 8). The Examiner stated, however, that Song discloses embedding the system in an integrated circuit (IC) and that Trimberger discloses a PLD integrated circuit. (Office Action, p. 8). The Examiner concluded that it would have been obvious to employ the PLD of Trimberger as the IC of Song in order to make use of programmable features of a PLD. (Office Action, p. 8).

Claims 16-18 depend from claim 15 and recite additional features therefor. As discussed above, Song does not teach or suggest a semaphore circuit and a "means

for controlling access among the plurality of processors to the first portion of the memory in response to a state of the semaphore circuit," as recited in claim 15. Rather, the principle of operation for the system in Song is to control access to a shared memory among the processors based on states of multiple lock buffers, one for each processor. Trimberger generally describes a PLD configured with an output register for specifying memory space during a reconfiguration operation. Trimberger is devoid of any teaching or suggestion of arbitrating access to a shared memory among a plurality of processors. Since neither Song nor Trimberger teach or suggest a means for controlling access among processors to a memory in response to a state of a semaphore circuit, no conceivable combination of Song and Trimberger renders obvious Applicants' invention recited in claim 15. Therefore, Applicants contend that Claims 16-18, which depend from Claim 15, are patentable over the combination of cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 5, 2005.

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Signature